Datasheet – MAP7101

Synchronous Boost Converter with Isolation FET

General Description

The MAP7101 is a 1.2MHz current mode step up regulator with built-in power switching MOSFET and isolation FET.

The MAP7101 step up regulator provides fast transient response to pulsed loads while producing efficiencies over 90%. A built-in programmable soft-start function limits inrush currents during start-up.

MAP7101 provides over load protection, over current protection, output over voltage protection, thermal shutdown, and under voltage lockout.
MAP7101 is available 10-pin DFN Package with Halogen-free (fully RoHS compliant).

RoHS Compliant
HALOGEN-FREE

Features

- Up to 90% efficiency synchronous boost
- 2.7V to 5.5V input voltage range
- 20V internal switch FET
- Integrated synchronous FET & isolation FET
- Fixed 1.2MHz Switching Frequency
- Programmable Soft Start
- Over Current Protection
- Over Load Protection with Isolation FET
- Over Voltage Protection
- Output Load Discharge Path After Shutdown
- Thermal shutdown
- UVLO
- DFN-10L Package with Halogen-free

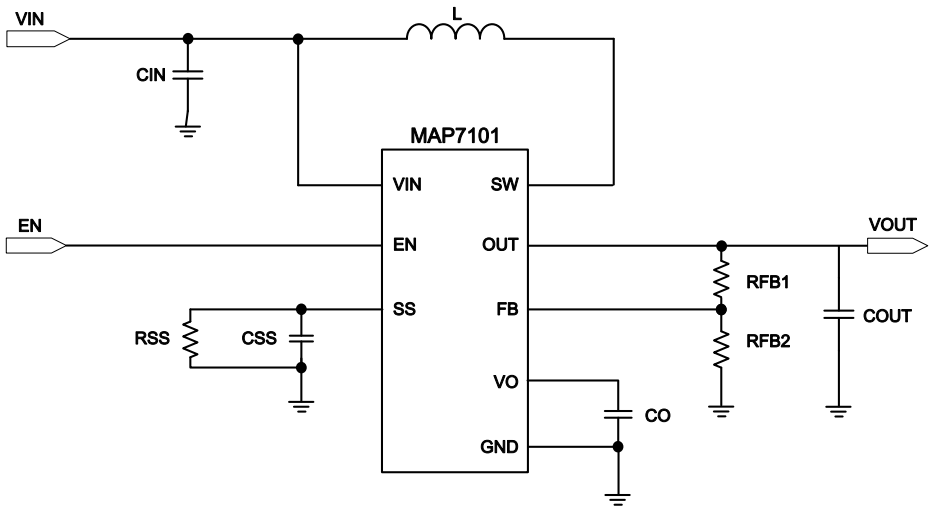
Applications

- SSD Power System
- OLED Power Supply

Ordering Information

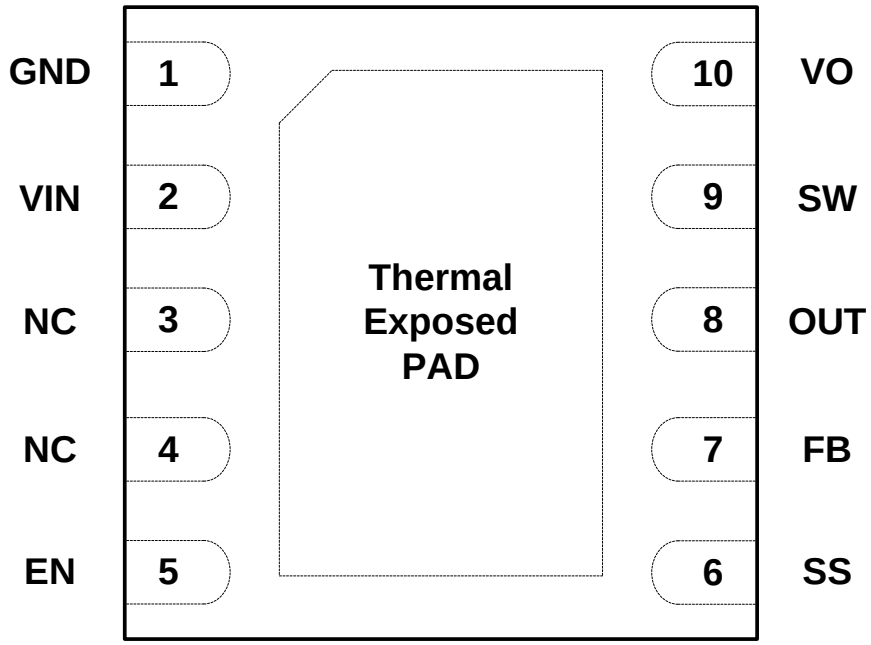
Part Number	Top Marking	Junction Temperature Range	Package	RoHS Status
MAP7101DFRH	MAP7101	-40℃ to +125℃	DFN-10L 2.5mm X 2.5mm	Compliant

Typical Application



Pin Configuration

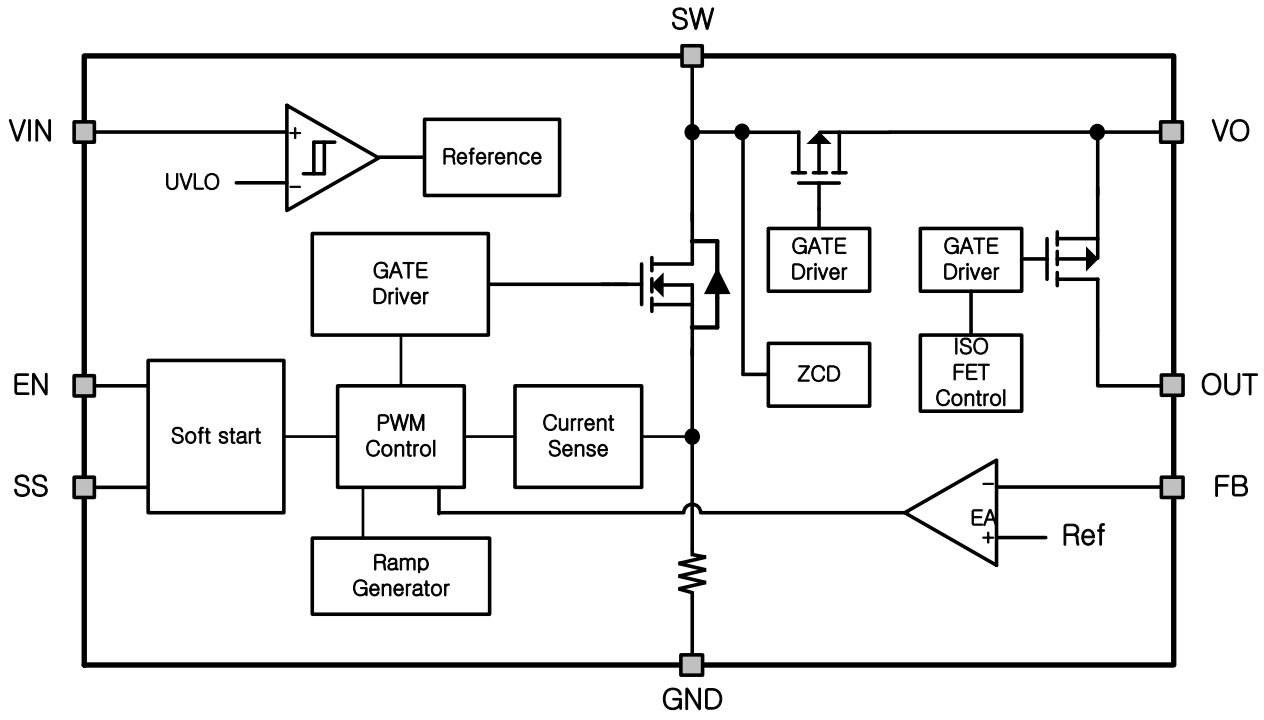
DFN-10L 2.5mm x 2.5mm
TOP View



Pin Description

DFN 10pin	Name	Description
1	GND	Ground.
2	VIN	Power supply input. Need external bypass capacitor.
3	NC	Not connect.
4	NC	Not connect.
5	EN	Enable pin.
6	SS	Soft start pin. RC network connect to the SS pin programs soft start timing.
7	FB	Output voltage feedback pin. An external resistor divider connected to this pin programs the regulated output voltage.
8	OUT	Isolation switch is between this pin and VO pin. Connect load to this pin for input/output isolation during IC shutdown.
9	SW	Switching node of the IC where the internal PWM switch operates.
10	VO	Output of the boost converter. When the output voltage exceeds the overvoltage protection (OVP) threshold, the power switch turns off until VO drops below the overvoltage protection hysteresis.

Functional Block Diagram



Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Min	Max	Unit
V_{VIN}, V_{EN}, V_{SS}	VIN, EN, SS pins Voltage	-0.3	6.0	V
V_{SW}, V_{VO}, V_{OUT}	SW, VO, OUT pins Voltage	-0.3	20	V
V_{FB}	FB pins Voltage	-0.3	3	V
T_J	Junction Temperature	-40	+150	°C
T_S	Storage Temperature	-65	+150	°C
ESD	HBM on All Pins (Note 2)	-2000	+2000	V
	CDM on All Pins (Note 3)	-200	+500	

Note 1: Stresses beyond the above listed maximum ratings may damage the device permanently. Operating above the recommended conditions for extended time may stress the device and affect device reliability. Also the device may not operate normally above the recommended operating conditions. These are stress ratings only.
Note 2: ESD tested per JESD22A-114.
Note 3: ESD tested per JESD22C-101.

Recommended Operating Conditions (Note 1)

Parameter		Min	Max	Unit
V_{VIN}	Supply Input Voltage	2.7	5.5	V
$V_{O/OUT}$	VO, OUT Output Voltage Range	V_{IN} + 0.5	13.5	V
T_J	Operating Junction Temperature	-40	125	°C

Note 1: Normal operation of the device is not guaranteed if operating the device over outside range of recommended conditions.

Package Thermal Resistance (Note 1)

Parameter		θ_{JA}	θ_{JC}	Unit
MAP7101	DFN-10L	49.2	7.6	℃/W

Note 1: Multi-layer PCB based on JEDEC standard (JESD51-7)

Electrical Characteristics

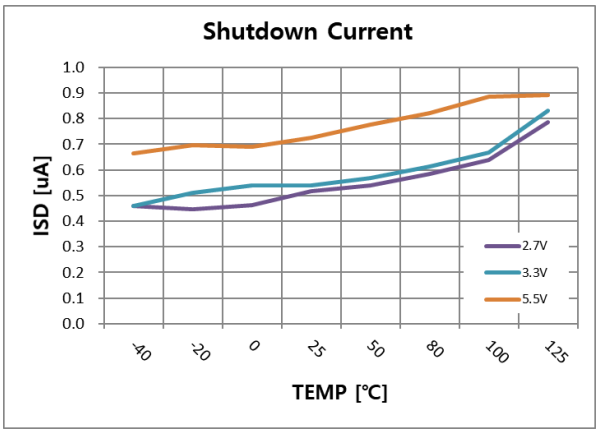
V_{IN} = 3.3V, C_{IN} = 10μF, T_A = -25°C to 85°C (Note 1), and typical values are tested at T_A = 25°C (unless otherwise noted)

Parameter		Test Condition	Min	Typ	Max	Unit
Supply						
V_{VIN}	Input Voltage Range		2.7		5.5	V
I_Q	Quiescent Current	No Switching, No Load, VFB>0.55V		0.7	1.3	mA
		Device PWM Switching, No load, excepted IL		0.9	1.5	mA
I_{SD}	Shutdown Current	V_{IN} = 5.5V, EN=GND			1	uA
V_{UVLO}	Under Voltage Lockout Threshold Voltage on VIN pin	Lockout threshold(Falling V_{VIN})	2.00	2.25	2.48	V
		Lockout hysteresis		150		mV
Enable Control						
V_{EN}	Logic Input Level on EN pins	V_{PWM_L} : Logic Low			0.3	V
		V_{PWM_H} : Logic High	1.2			
R_{EN}	Pull-down Resistor on EN pins	V_{PWM} = 4V	400	800	1600	kΩ
t_{OFF}	EN pulse width to shutdown	EN high to low			1	ms
Voltage Control						
V_{REF}	Voltage feedback regulation		0.49	0.5	0.51	V
I_{FB}	Voltage feedback input bias current				100	nA
f_S	Oscillator frequency		1.0	1.2	1.4	MHz
D_{max}	Maximum duty cycle (Note 1)	V_{FB} = 0.1 V, T_A = 85°C	90	93		%
T_{min_on}	Minimum on pulse width (Note 1)			65		ns
T_{SS}	Soft start time (Note1) (Note2)	EN High to VOUT 95%; C_{SS} = 10nF, R_{SS} = 200kΩ, C_{FF} = Open		1.25		ms
Power Switch, Isolation FET						
$R_{DS(ON)N}$	N-channel MOSFET on-resistance	V_{IN} = 3.3 V		0.2		Ω
$R_{DS(ON)P}$	P-channel MOSFET on-resistance	V_{IN} = 3.3 V		0.6		Ω
$R_{DS(ON)ISO}$	Isolation FET on-resistance	V_{VO} = 12 V		2		Ω
		V_{VO} = 5 V (Note 1)		3		
I_{LN_N}	N-channel leakage current	V_{DS} = 20 V, T_A = 25°C			1	uA
I_{LN_iso}	Isolation FET leakage current	V_{DS} = 20 V, T_A = 25°C			1	uA
Protection						
I_{OCP}	N-Channel MOSFET current limit		1.05	1.4	1.9	A
V_{OVP}	Over voltage protection threshold	VO pin	14	14.5		V
V_{OVP_hys}	Over voltage protection hysteresis			1.0		V
I_{OLP}	Over load protection		200	350		mA
TSD	Thermal shutdown threshold (Note 1)			150		°C
TSD_{hys}	Thermal shutdown hysteresis (Note 1)			15		°C

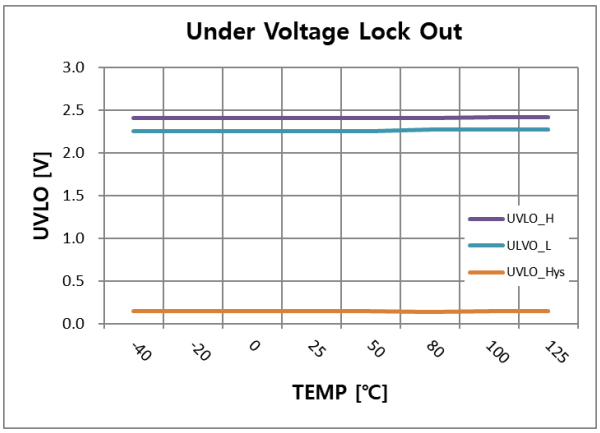
Note 1: These parameters, although guaranteed by design, are not tested in mass production.
Note 2: The criteria for measuring soft start time are as follows. EN high to V_{SS} 95% (same as V_{OUT} 95%) at condition C_{SS}=10nF, R_{SS}=200kΩ, C_{FF}=Open.

Typical Operating Characteristics

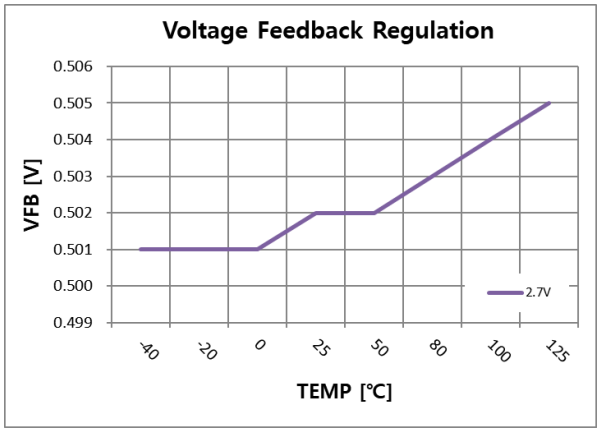
[ISD vs Temperature]



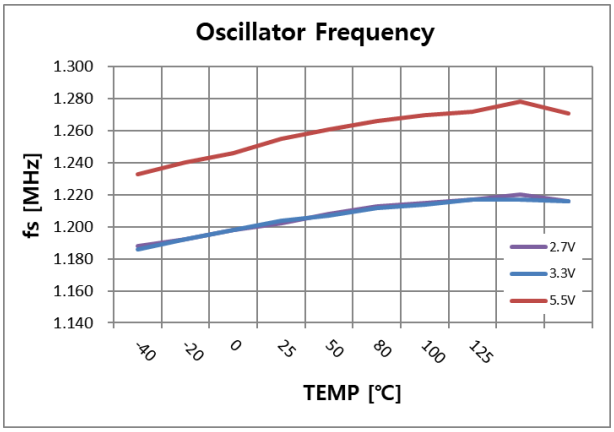
[UVLO vs Temperature]



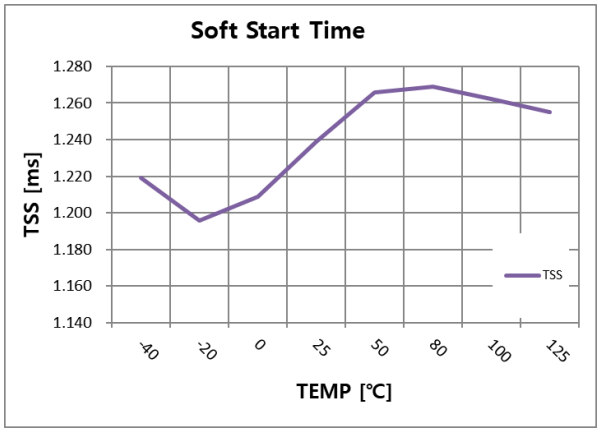
[VFB vs Temperature]



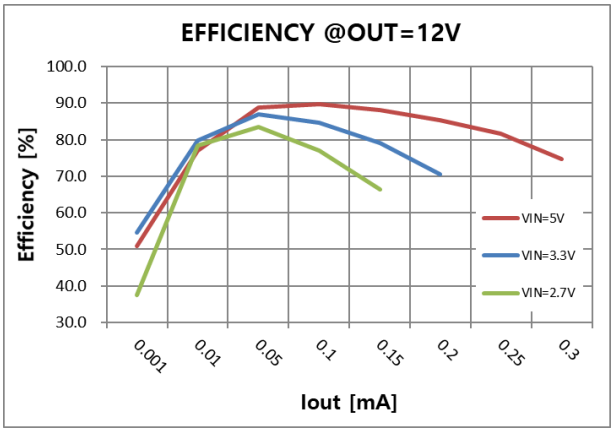
[fs vs Temperature]



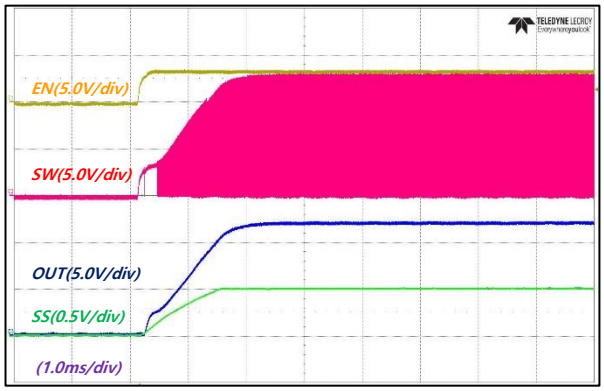
[TSS vs Temperature]



[Efficiency vs Load]

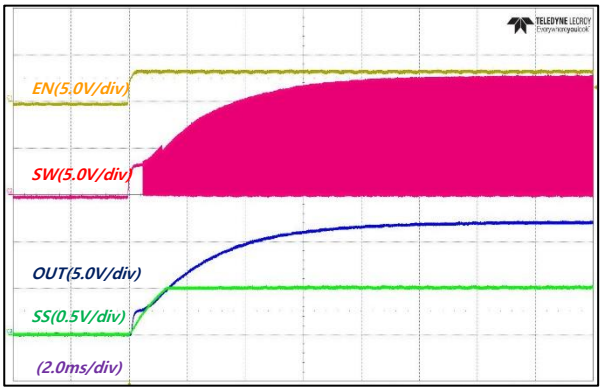


[Soft Start-up]



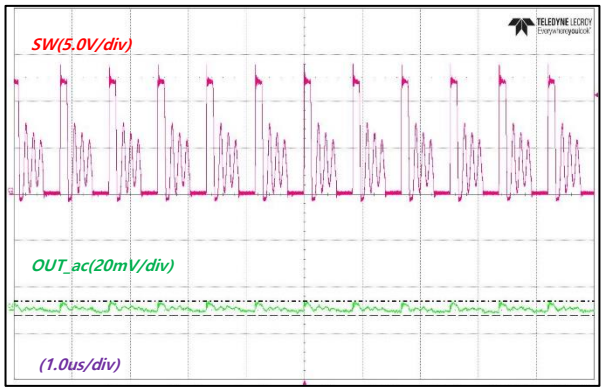
VIN=3.3V, VOUT=12V, IOUT=100mA, Cff=1nF

[Soft Start-up]



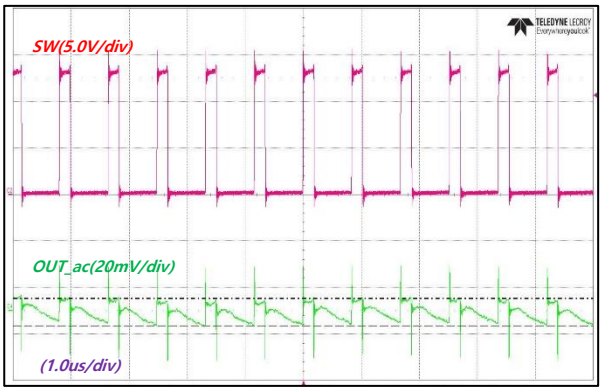
VIN=3.3V, VOUT=12V, IOUT=100mA, Cff=10nF

[Switching Waveform in DCM]



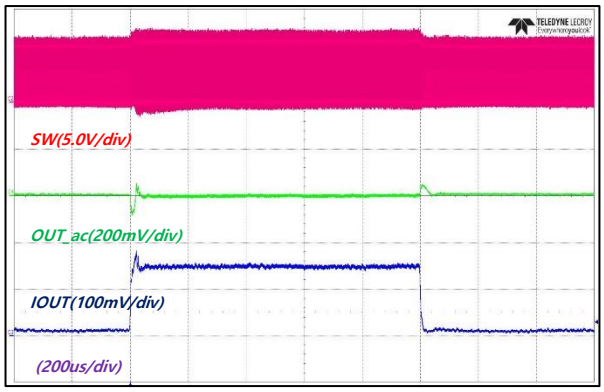
VIN=3.3V, VOUT=12V, IOUT=10mA, Cff=10nF

[Switching Waveform in CCM]



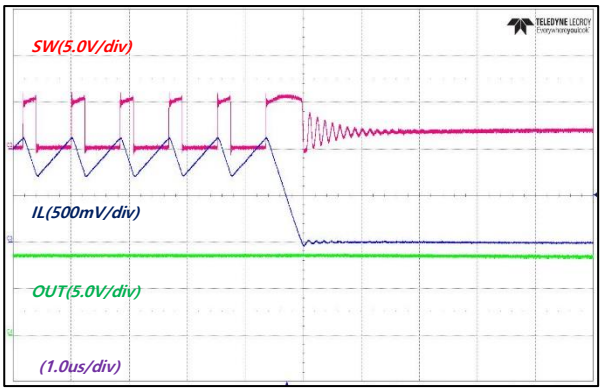
VIN=3.3V, VOUT=12V, IOUT=150mA, Cff=10nF

[Load Transient Response]



VIN=3.3V, VOUT=12V, IOUT=10-150mA, Cff=10nF

[Over Load Protection]



VIN=3.3V, VOUT=12V, IOUT=250mA, Cff=10nF

Functional Description

The MAP7101 is a 1.2MHz, synchronous, highly integrated step-up converter with true output disconnect. The MAP7101 integrates an N-channel and a P-channel MOSFET to synchronous rectifier. Replacing the traditional Schottky diode with a low Rds(on) P-MOS improves efficiency.

This IC also integrates an output-side isolation switch as shown in the functional block diagram. One common issue with conventional boost regulators is the conduction path from input to output even when the PWM switch is turned off. It creates three problems, which are inrush current during start-up, output leakage current during shutdown, and excessive overload current. In the MAP7101, the isolation switch turns off under shutdown-mode and overload conditions, thereby opening the current path. However, shorting the VO and OUT pins bypasses the isolation switch and enhances efficiency.

Shutdown and Load Discharge

When the EN pin is pulled low for 1ms, the IC stops the PWM switch, synchronous switch and turns off the isolation switch, providing isolation between input and output. The isolation switch offed and then fast discharge FET is quickly discharges the output voltage until threshold voltage. Afterwards, the voltage is slowly discharged to zero by the leakage current.

Also when the UVLO is low, the output voltage fast discharges operation. This protects the IC and the external components from high voltage in shutdown mode. In shutdown mode, less than 1μA of input current is consumed by the IC.

UVLO

An under voltage lockout prevents improper operation of the device for input voltages below 2.4V. When the input voltage is below the under voltage threshold, the entire device, including the PWM and isolation switches, remains off.

Overload and Overvoltage Protection

If the overload current passing through the isolation switch is above the overload limit typical 300mA, the MAP7101 is shut-down until the fault is cleared and the EN pin toggles. These operating to prevent the PWM switch and the output capacitor from exceeding maximum voltage ratings, an overvoltage protection circuit turns off the boost switch as soon as the output voltage at the VO pin exceeds the OVP threshold.

Thermal Shutdown Detection

An internal thermal shutdown turns off the isolation and PWM switches when the typical junction temperature of 150°C is exceeded. The thermal shutdown has a hysteresis of typical 15°C.

Device Functional Modes

The converter operates in continuous conduction mode (CCM) as soon as the input current increases above half the ripple current in the inductor, for lower load currents it switches into discontinuous conduction mode (DCM). If the load is further reduced, the part starts to skip pulses to maintain the output voltage.

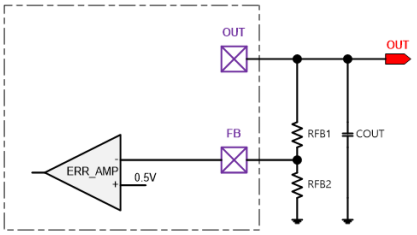
Application Information

The device is a step up DC-DC converter with a PWM switch, a power synchronous rectifier switch and an input/output isolation switch integrated. MAP7101 supports up to 13.5V output with the input range from 2.7V to 5.5V. The MAP7101 adopts the current-mode control with constant pulse-width-modulation (PWM) frequency. The switching frequency is fixed at 1.2 MHz typical. The isolation switch disconnects the output from the input during shutdown to minimize leakage current. However, shorting the VO and OUT pins bypasses the isolation switch and enhances efficiency.

Output Voltage Program

Output voltage can be set by feeding back the output to the FB pin using a resistor divider network as shown in Figure below. The resistor divider network includes RFB1 and RFB2. Usually, a design is started by picking a fixed R2 value and calculating the required R1 with the equation below:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_{FB1}}{R_{FB2}}\right) \text{..... (1)}$$

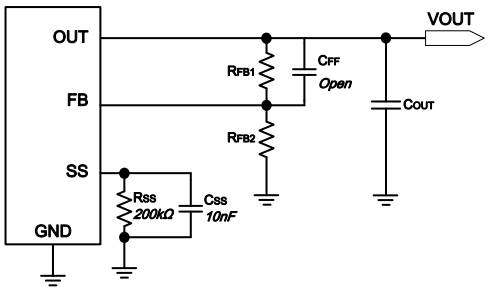


Soft Start Time

The MAP7101 turn on isolation FET and PWM switch when the EN pin is pulled high. During the soft start period, the R and C network on the SS pin is charged by an internal bias current of 5uA. The R and C network sets the reference voltage rise time follows the SS pin voltage until the SS pin voltage reaches 0.5V. The soft start time is given as follows Simple Equation without RSS:

$$t_{SS} = \frac{0.5V \times C_{SS}}{5uA}$$

Where, CSS is the 10nF capacitor and CFF is open condition.



When the EN pin is pulled low to switch the IC off, the SS pin voltage is discharged to zero by the resistor RSS 200kΩ. The discharge period depends on the RC time constant. Note that if the SS pin voltage is not discharged to zero before the IC is enabled again, the soft start circuit may not slow the output voltage startup and may not reduce the startup inrush current

Switching Duty Cycle (D)

The maximum switch duty cycle of the MAP7101 is 90% minimum. The duty cycle of a boost converter under continuous conduction mode (CCM) is given by:

$$D_{UTY} = \frac{V_{OUT} + V_{OUT} - V_{IN}}{V_{OUT} + 0.8V}$$

The duty cycle must be lower than the specification in the application; otherwise the output voltage cannot be regulated.

The MAP7101 has a minimum ON pulse width once the PWM switch is turned on. As the output current drops, the device enters discontinuous conduction mode (DCM). If the output current drops extremely low, causing the ON time to be reduced to the minimum ON time, the MAP7101 enters pulse-skipping mode. In this mode, the device keeps the power switch off for several switching cycles to keep the output voltage in regulation. The output current when the IC enters skipping mode is calculated as follows Equation:

$$I_{OUT\_PSM} = \frac{V_{IN}^{\ 2} \times T^{2}_{MIN\_ON} \times f_{SW}}{2 \times (V_{OUT} + 0.8V - V_{IN}) \times L}$$

Where, T_{MIN_ON} = Minimum On pulse width specification
L = Selected Inductor Value
f_{SW} = Converter Switching Frequency

Inductor Selection

The inductor is used to supply constant current to output when it is driven by a switching voltage. For given input and output voltage, inductance and switching frequency together decide the inductor ripple current, for most designs, the inductance value can be derived from the following equation:

$$I_{L\_PEAK} = I_{L\_DC} + \frac{\Delta I_L}{2}$$

$$I_{L\_DC} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta}$$

$$\Delta I_L = \frac{1}{L \times f_{SW} \times \left(\frac{1}{V_{OUT} + 0.8V - V_{IN}} + \frac{1}{V_{IN}} \right)}$$

Where, I_{L_PEAK} = Peak Switch Current
I_{L_DC} = Inductor Average Current
ΔI_L = Inductor Peak to Peak Current
η = Estimated Converter Efficiency

Normally, it is advisable to work with an inductor peak-to-peak current of less than 30% of the average inductor current. A smaller ripple from a larger valued inductor reduces the magnetic hysteresis losses in the inductor and EMI. But in the same way, load transient response time is increased. Also, the inductor value should not be outside the 2.2μH to 10μH range in the recommended operating conditions table. Otherwise, the internal slope compensation and loop compensation components are unable to maintain small signal control loop stability over the entire load range.

Input and Output Capacitor Selection

The output capacitor is mainly selected to meet the requirements for output ripple and loop stability. This ripple voltage is related to the capacitor's capacitance and its equivalent series resistance (ESR). Assuming a ceramic capacitor with zero ESR, the minimum capacitance needed for a given ripple can be calculated by:

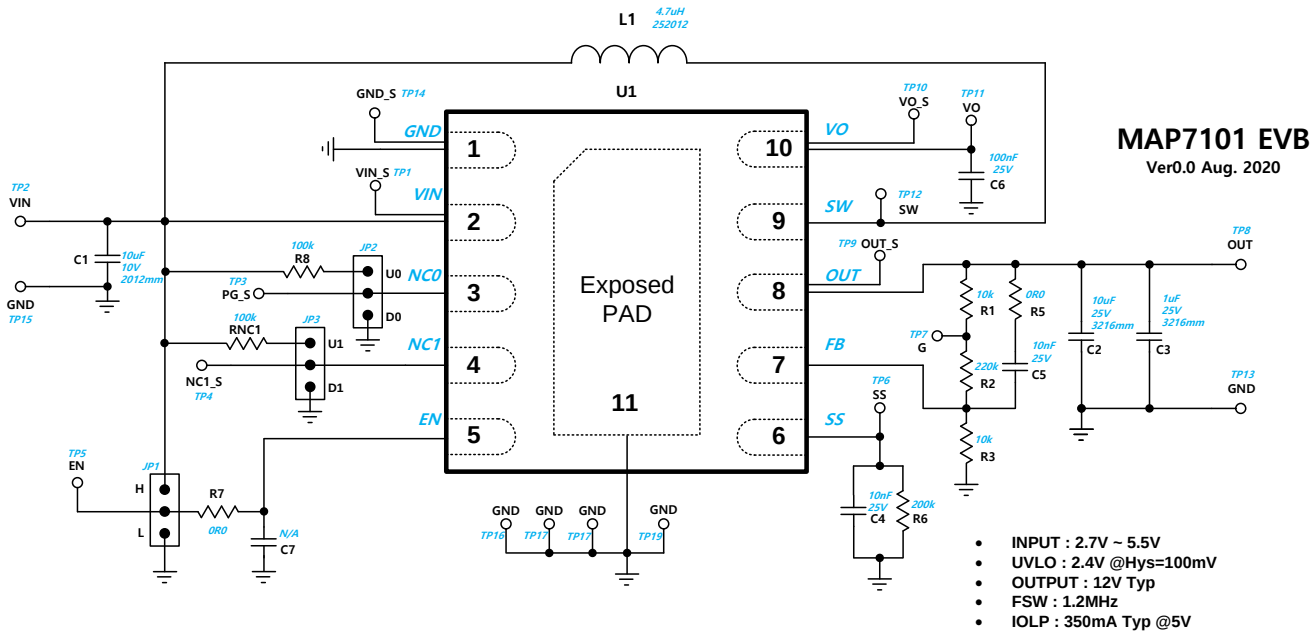
$$C_{OUT} = \frac{D \times I_{OUT}}{f_{SW} \times V_{RIPPLE}}$$

Where, V_{RIPPLE} = Peak to Peak Output Ripple

The ESR impact on the output ripple must be considered if tantalum or electrolytic capacitors are used. Care must be taken when evaluating a ceramic capacitor's derating under dc bias, aging, and ac signal. For example, larger form factor capacitors (in 1206 size) have their self-resonant frequencies in the range of the switching frequency. So the effective capacitance is significantly lower. The dc bias can also significantly reduce capacitance. A ceramic capacitor can lose as much as 50% of its capacitance at its rated voltage. Therefore, always leave margin on the voltage rating to ensure adequate capacitance at the required output voltage. Input capacitor 4.7uF_mininum is recommended. The output requires a capacitor in the range of 1μF to 10μF.

The output capacitor affects the small signal control loop stability of the boost regulator. If the output capacitor is below the range, the boost regulator can potentially become unstable.

Application Circuit



Symbol	Vender	Part Number	Value
L1	ABCO	LPP252012-S	Chip Inductor, 4.7uH, ±20%, 0.24Ω, 2.7A_Typ, 252012mm
L1	Murata	DFE252012F-4R7M	Chip Inductor, 4.7uH, ±20%, 0.19Ω, 2.1A_Typ, 252012mm
C1	SEMCO	CL10A106MO8NNN	Capacitor Ceramic, 10uF, ±20%, 16V, X5R, 1608mm
C2	SEMCO	CL10A106MA8NRN	Capacitor Ceramic, 10uF, ±20%, 25V, X5R, 1608mm
C3	SEMCO	CL10A105KA8NNN	Capacitor Ceramic, 1uF, ±10%, 25V, X5R, 1608mm
C4	SEMCO	CL10A103KA8NNN	Capacitor Ceramic, 10nF, ±10%, 25V, X5R, 1608mm
C5	SEMCO	CL10A103KA8NNN	Capacitor Ceramic, 10nF, ±10%, 25V, X5R, 1608mm
C6	SEMCO	CL10A104KA8NNN	Capacitor Ceramic, 100nF, ±10%, 25V, X5R, 1608mm
R1, R3	SEMCO	RC1608F103CS	Chip Resistor, 10kΩ, ±1%, 1/10W, 50V, 1608mm
R2	SEMCO	RC1608F224CS	Chip Resistor, 220kΩ, ±1%, 1/10W, 50V, 1608mm
R5, R7	SEMCO	RC1608F0R0CS	Chip Resistor, 0Ω, ±1%, 1/10W, 50V, 1608mm
R6	SEMCO	RC1608F204CS	Chip Resistor, 200kΩ, ±1%, 1/10W, 50V, 1608mm

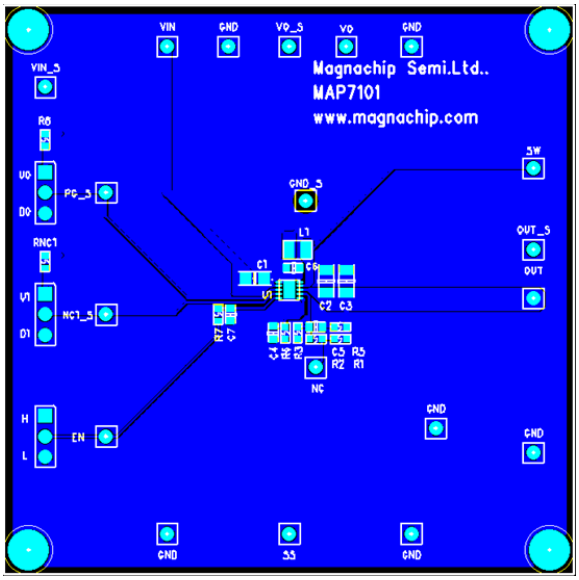
PCB Layout Guide

Layout is important, especially for switching power supplies with high switching frequencies; poor layout results in reduced performance, EMI problems, resistive loss, and even system instability.

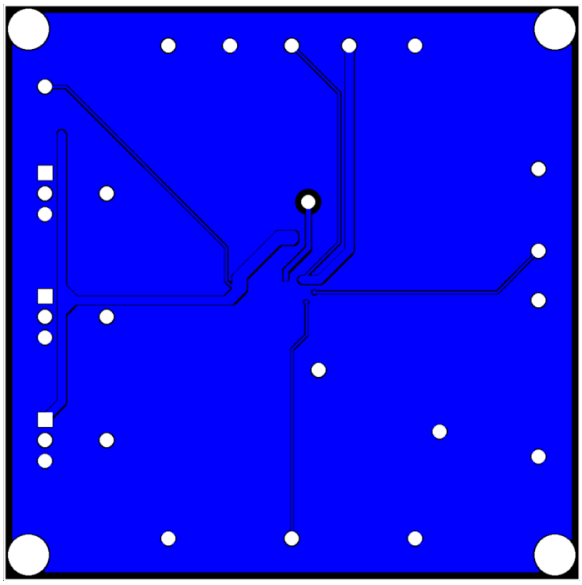
- Place a decoupling capacitor as close as possible from OUT to GND and a short and wide trace between the OUT pin and the output capacitor to reduce spikes on the SW node and improve EMI performance.
- Place the input capacitor, output capacitor, and inductor as close to the IC as possible with a short and wide trace.
- Place the feedback divider resistors as close as possible to the signal control GND trace.
- Use a large copper GND area to lower the die temperature by expose pad.

Figure shows the recommended component placement for the MAP7101.

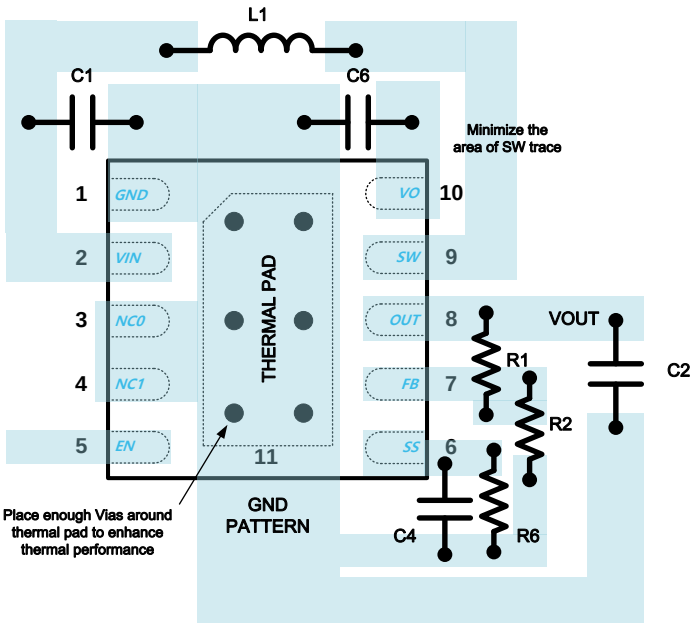
[TOP Side Layout]



[BOTTOM Side Layout]

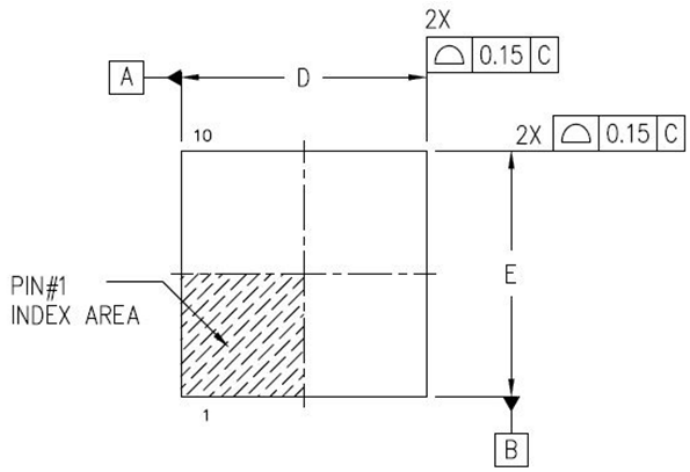


[MAP7101 Layout Guide]

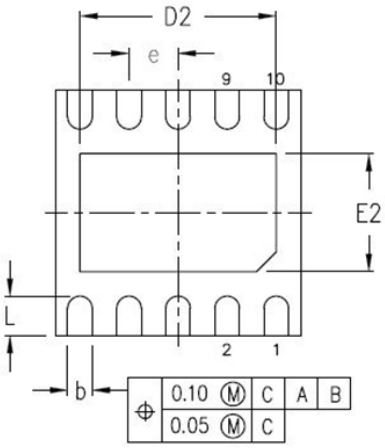


PKG Dimensions

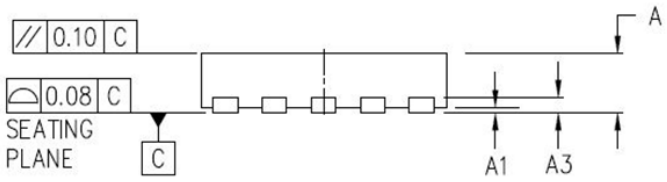
DFN-10L 2.5mm x 2.5mm x 0.55mm



TOP VIEW



BOTTOM VIEW



SIDE VIEW

Symbol	Dimsion (mm)		
	Min	Nom	Max
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A3		0.15 REF.	
D	2.40	2.50	2.60
E	2.40	2.50	2.60
D2	1.90	2.00	2.10
E2	1.10	1.20	1.30
b	0.20	0.25	0.30
e		0.50 BSC	
L	0.35	0.40	0.45

NOTES :

1. Reference JEDEC MO-229
2. The configuration of PIN #1 identifier is optional

Datasheet Revision History

Date	Version	Changes
2019-11-05	Version 0.0	Initial release
2020-02-18	Version 0.1	Changed to P-CH MOSFET instead of internal power diode Changed to T_A to T_J
2020-03-06	Version 0.2	Add PKG Dimensions (thickness=0.55mm @0.8mm Competitor)
2020-06-18	Version 0.0	Preliminary datasheet initial release Add to condition Ta=-25℃to 85℃ by Note1
2021-04-14	Version 0.1	Changed to typo I_{OCP}=1.1A/1.2A/1.5A → 0.9A/1.1A/1.5A Changed to OLP level 300mA → 350mA Add Note1 → T_{MIN_ON}, Isolation FET on-resistance V_{VO}=5V
2021-04-28	Version 0.2	Changed I_{OCP}=0.9A/1.1A/1.5A → 1.05A/1.4A/1.9A (OCP-3 up trim)
2021-05-21	Version 0.3	Updated IQ, Rthja, Rthjc Changed to typo UVLO Condition Add to Layout Guide
2021-06-19	Version 1.0	Add to IQ, TSS Changed to UVLO Low Condition, OVP Hys.